

PCR – Motion Status Register (command/status, R/W)

PCR is a 16-bit command and status register, containing both masks and status information for TML protections.

TML Address: 0x0303

Contents. PCR information is structured as follows:

15	14	13	12	11	10	9	8
I2DPRS	EBWPRS	UVPRS	OVPRS	OT2PRS	OT1PRS	I2TMPRS	IMXPRS
0	0	0	0	0	0	1	0
7	6	5	4	3	2	1	0
I2DPRM	EBWPRM	UVPRM	OVPRM	OT2PRM	OT1PRM	I2TMPRM	IMXPRM
0	0	0	0	0	0	0	0

Bit 15 I2DPRS. Status of drive i2t protection

- 0 = Not triggered
- 1 = Triggered

Bit 14 EBWPRS. Status of encoder broken wire protection

- 0 = Not triggered
- 1 = Triggered

Bit 13 UVPRS. Status of under voltage protection

- 0 = Not triggered
- 1 = Triggered

Bit 12 OVPRS. Status of over voltage protection

- 0 = Not triggered
- 1 = Triggered

Bit 11 OT2PRS. Status of drive over temperature protection

- 0 = Not triggered
- 1 = Triggered

Bit 10 OT1PRS. Status of motor over temperature protection

- 0 = Not triggered
- 1 = Triggered

Bit 9 I2TMPRS. Status of motor i2t protection

- 0 = Not triggered
- 1 = Triggered

Bit 8 IMAXP. Status of over current protection

- 0 = Not triggered
- 1 = Triggered

Bit 7 I2DPRM. Mask for drive I2t protection

- 0 = Disable
- 1 = Enable

Bit 6 EBWPRM. Mask for encoder broken wire protection

- 0 = Disable
- 1 = Enable

Bit 5 UVPRM. Mask for under voltage protection

- 0 = Disable
- 1 = Enable

Bit 4 OVPRM. Mask for over voltage protection

- 0 = Disable
- 1 = Enable

Bit 3 OT2PRM. Mask for drive over temperature protection

- 0 = Disable
- 1 = Enable

Bit 2 OT1PRM. Mask for motor over temperature protection

- 0 = Disable
- 1 = Enable

Bit 1 I2TPRM. Mask for motor I2t protection

- 0 = Disable
- 1 = Enable

Bit 0 IMXPRM. Mask for maximum current protection

- 0 = Disable
- 1 = Enable